In re Patent Application of:
MORIN ET AL.
Serial No. **10/701,165**
Filing Date: **November 4, 2003**

In the Claims:

Claims 1-11 (Cancelled).

12. (Currently amended) A semiconductor device comprising:

a semiconductor substrate;

at least one ~~first MOS~~ PMOS transistor and at least one ~~second MOS~~ NMOS transistor in said semiconductor substrate;

a dielectric layer on said at least one ~~first MOS~~ PMOS transistor and on said at least one ~~second MOS~~ NMOS transistor; and

a first etch-stop layer covering said at least one ~~first MOS~~ PMOS transistor and having a first residual stress level; and

a second etch-stop layer covering said at least one ~~first MOS~~ PMOS transistor and said at least one ~~second MOS~~ NMOS transistor and having a second residual stress level different than the first residual stress level;

said first etch-stop layer having a negative residual stress level above said at least one PMOS transistor, and said second etch-stop layer having a positive residual stress level above said at least one NMOS transistor.

13. (Previously presented) A semiconductor device according to Claim 12, wherein said first and second etch-stop layers have different thicknesses.

14. (Currently amended) A semiconductor device according to Claim 12, wherein said dielectric layer includes

contact openings therethrough for providing electrical connection to said at least one ~~first MOS~~ PMOS transistor and to said at least one second MOS transistor.

15. (Cancelled).

16. (Cancelled).

17. (Cancelled).

18. (Cancelled).

19. (Previously presented) A semiconductor device according to Claim 12, wherein a zone formed by said second etch-stop layer overlapping said first etch-stop layer has a substantially zero residual stress level.

20. (Cancelled).

21. (Cancelled).

22. (Cancelled).

23. (Cancelled).

24. (Cancelled).

25. (Cancelled).

26. (Cancelled).

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27. (Cancelled).

28. (Cancelled).

29. (Cancelled).

30. (Cancelled).

31. (Cancelled).

32. (Currently amended) A method for fabricating a semiconductor device comprising:

forming at least one ~~first MOS~~ PMOS transistor and at least one ~~second MOS~~ NMOS transistor in a semiconductor substrate;

forming a dielectric layer on the at least one ~~first MOS~~ PMOS transistor and on the at least one ~~second MOS~~ NMOS transistor; ~~and~~

forming a first etch-stop layer covering the at least one ~~first MOS~~ PMOS transistor and having a first residual stress level; and

forming a second etch-stop layer covering the at least one ~~first MOS~~ PMOS transistor and the at least one ~~second MOS~~ NMOS transistor and having a second residual stress level different than the first residual stress level;

the first etch-stop layer having a negative residual stress level above the at least one PMOS transistor, and the second etch-stop layer having a positive residual stress level above the at least one NMOS transistor.

33. (Previously presented) A method according to Claim 32, wherein the first and second etch-stop layers have different thicknesses.

34. (Currently amended) A method according to Claim 32, further comprising forming contact openings through the dielectric layer for providing electrical connection to the at least one ~~first MOS~~ PMOS transistor and to the at least one ~~second MOS~~ NMOS transistor.

35. (Currently amended) A method according to Claim 32, wherein forming the first etch stop layer comprises:

forming the first etch-stop layer covering the at least one ~~first MOS~~ PMOS transistor and the at least one ~~second MOS~~ NMOS transistor;

forming a mask on the at least one ~~first MOS~~ PMOS transistor;

removing the first etch-stop layer on the at least one ~~second MOS~~ NMOS transistor; and

removing the mask.

36. (Currently amended) A method according to Claim 32, further comprising performing a localized treatment of the first and second etch-stop layers that overlap the at least one ~~first MOS~~ PMOS transistor for modifying the second residual stress level of the second layer.

37. (Previously presented) A method according to Claim 36, wherein performing the localized treatment comprises

implanting ions into the second etch-stop layer.

38. (Previously presented) A method according to Claim 37, wherein germanium ions are implanted into the second etch-stop layer.